REMARKS

The Official Action dated November 27, 2006 has been received and its contents carefully noted. In view thereof, it is respectfully requested that the objections and rejections of record be reconsidered and withdrawn by the Examiner in view of the following detailed comments. As previously, claims 1-14 are presently pending in the instant application.

Initially, Applicant wishes to acknowledge the Examiner's indication in paragraph 6 of the Office Action that claims 11-14 contain allowable subject matter and would be allowed if rewritten to include all of the limitations of the base claim and any intervening claims. For the following reasons, It is respectfully submitted that Independent claim 1 clearly distinguishes over the prior art of record and is in proper condition for allowance. Accordingly, it is respectfully requested that claims 11-14 again be indicated as being allowable over the prior art of record along with the all other claims presently pending in the instant application.

Turning now to paragraph 1 of the Official Action, claims 1-5 and 10 have been rejected under 35 U.S.C. §102(b) as being anticipated by Pan (U.S. Patent No. 6,348,823 hereafter Pan). This rejection is respectfully traversed in that the patent to Pan neither discloses or suggests that which is presently set forth by Applicant's claimed invention.

As set forth in the previous amendments to independent claim 1, this claim recites a phase adjustment circuit that receives a first pair of clock signals and outputs a second pair of clock signals with phases satisfying a predetermined condition to a central processing unit, comprising a clock proliferator that receives a first clock signal and generates a plurality of clock signals therefrom, a clock selector that receives said plurality of clock signals from the clock proliferator, selects one of the received plurality of clock signals in accordance with a selection signal, and outputs the selected clock signal, and a phase difference detector that receives the selected clock signal and a second clock signal differing in frequency from the first clock signal and the selected clock signal, determines whether the phase of the second clock signal and the phase of the selected clock signal satisfy the predetermined condition, and outputs a detection signal indicating whether the predetermined condition is satisfied, with the first clock signal and the second clock signal constituting the first pair of clock signals and the second clock signal and the selected clock signal constituting the second pair

of clock signals. That is, the present invention as set forth in independent claim 1, outputs two clock signals (the second clock signal and the selected clock signal) with different frequencies for use by a CPU. The purpose of the circuit as set forth in independent claim 1 is to serve the needs of a CPU that requires two clock signals with different frequencies but a predetermined phase relationship. The claimed circuit operates by receiving two clock signals with different frequencies and adjusting the phase of one of the two signals in order to obtain the necessary phase relationship.

More specifically, independent claim 1 recites a circuit that receives a pair of clock signals with different frequencies, a first clock signal and a second clock signal, and recites that the second clock signal differs in frequency from the first clock signal and outputs a pair clock signals with different frequencies, the second clock signal and a selected clock signal. Independent claim 1 further recites that the second clock signal differs in frequency from the selected clock signal. Clearly, these features are neither disclosed in or suggested by the teachings of Pan as Pan teaches a digital controlled oscillator that outputs a single signal, marked S_O in Fig. 7A and also denoted by reference numeral 710.

In reviewing the Pan disclosure, it is noted that Pan's digital controlled oscillator receives a single clock signal (702) and outputs a single clock signal (710 or S_O). The digital controlled oscillator operates by dividing the frequency of the input clock signal and delaying the divided signal by a selectable amount. Part of the digital controlled oscillator is a phase-frequency detector (PFD) 612 that compares the output clock signal (710) with a target clock signal (708), which Pan's circuit generates internally, but these two clock signals (708 and 710) have the same frequency, as can be readily seen by counting pulses in Fig. 7B. Further, as confirmation of this, in lines 58-59 of column 9, Pan states that the target clock has the same average frequency as the requirement, that is, the same average frequency as required in the output clock signal. In order to generate an output clock signal with a regular frequency and phase; however, Pan's circuit shifts the phase of the target clock 708 back and forth, making it irregular as shown in Fig. 7B.

In rejecting Applicant's claimed invention, the Examiner states that Pan's circuit would be fully capable or providing clocks (708 and 710) to a CPU; however, as the Examiner can readily appreciate, the irregular waveform of clock 708 would be disadvantageous for a CPU. Since clock 708 has the same frequency as clock 710, it is

difficult to ascertain what a CPU, which requires regularly-spaced clock pulses to operate properly, would gain by receiving the internal irregular target clock 708 as well as the intended regular output clock 710. Consequently, it is respectfully submitted that the patent to Pan fails to disclose or suggest that which is presently set forth by Applicant's claimed invention. Accordingly, it is likewise respectfully submitted that claim 1 as well as those claims which depend therefrom distinguish over the teachings of Pan and are in proper condition for allowance.

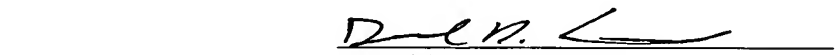
Turning now to paragraphs 2 and 3 of the Official Action, claims 6, 8 and 9 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Pan in view of Kuwata (U.S. Patent No. 6,959,061 hereinafter Kuwata) while claim 7 has also been rejected under 35 U.S.C. §103(a) as being unpatentable over Pan in view of Kuwata . These rejections are likewise respectfully traversed in that the patent Kuwata does nothing to overcome the aforementioned shortcomings associated with the teachings of Pan. That is, the patent to Pan, when taken alone or in view of the teachings of Kuwata, neither discloses or suggests that which is presently set forth by Applicant's claimed invention.

While the patent to Kuwata may disclose a phase detection circuit comprising a first flip-flop, a second flip-flop and a logic circuit for performing a logic operation on outputs of the first flip-flop and the second flip-flop thereby generating a detection signal (ESPD) that is held at a fixed value to prevent erroneous synchronization, this reference fails to overcome the aforementioned shortcomings discussed hereinabove with respect to the teachings of Pan. Particularly, Kuwata clearly fails to teach, disclose or suggest a phase difference detector that receives the selected clock signal and a second clock signal differing in frequency from the first clock signal and the selected clock signal, determines whether the phase of the second clock signal and the phase of the selected clock signal satisfy the predetermined condition, and outputs a detection signal indicating whether the predetermined condition is satisfied, as recited in independent claim 1. Accordingly, in that each of claims 6, 7, 8 and 9 are either directly or indirectly dependent upon independent claim 1 and include all of the limitations thereof, these claims are likewise believed to be in proper condition for allowance.

Therefore, in view of the foregoing, it is respectfully requested that the objections and rejections of record be reconsidered and withdrawn by the Examiner, that claims 1-14 be allowed and that the application be passed to issue.

Should the Examiner believe that a conference would be of benefit in expediting the prosecution of the instant application, the Examiner is hereby invited to telephone the undersigned to arrange such a conference.

Respectfully submitted,



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